

# TRANSMITTAL FORM

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<b>Application No.</b>	<b>10/656,628</b>		
	<b>Filing Date</b>	<b>September 5, 2003</b>	
	<b>First Named Inventor</b>	<b>Yoshihide SENZAKI</b>	
	<b>Examiner Name</b>	<b>Not yet assigned</b>	
	<b>Group Art Unit</b>	<b>2812</b>	
<b>Total Number of Pages in This Submission</b>	<b>6</b>	<b>Attorney Docket No.</b>	<b>A-71730/MSS (463035-878)</b>

## ENCLOSURES (check all that apply)

<input type="checkbox"/> Fee Transmittal Form	<input type="checkbox"/> Assignment Papers (for an Application)	<input type="checkbox"/> After Allowance Communication to Group
<input type="checkbox"/> Fee Attached	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences
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<input type="checkbox"/> Response to Missing Parts/ Incomplete Application	Remarks	
<input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53		

## SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Maria S. Swiatek, Esq., Reg. No. 37,244 DORSEY & WHITNEY LLP 4 Embarcadero Center, Suite 3400 San Francisco, CA 94111 Telephone : 650-494-8700	Customer Number 32940
Signature		
Date	March 15, 2004	

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Typed or printed name	Kari Bateman		
Signature		Date	March 15, 2004



PATENT  
Attorney Docket No. A-71730/MSS  
Dorsey File No. 463035-878

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

SENZAKI et al.

U.S. Serial No.: 10/656,628

Filing Date: September 5, 2003

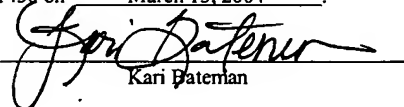
For: *Low Temperature Deposition of Silicon  
Based Thin Films by Single-Wafer Hot-Wall  
Rapid Thermal Chemical Vapor Deposition*

Examiner: Not yet assigned

Art Unit: 2812

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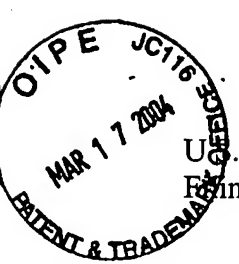
INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In satisfaction of the duty of disclosure under 37 C.F.R. § 1.56, and in accordance with the provisions of 37 C.F.R. §§ 1.97 and 1.98, Applicants wish to draw the attention of the U.S. Patent and Trademark Office to the references cited on the accompanying form PTO/SB/8A. In accordance with 1273 Off. Gaz. Pat. Off. 1, 8/5/2003, no copies of U.S. patents and U.S. published applications are enclosed. Copies of all other references are enclosed.

None of the foregoing references is believed to disclose the invention as claimed. Nothing herein shall constitute an admission concerning the contents of any of the cited references, nor shall the inclusion of a reference herein be considered an admission that the reference constitutes prior art against the invention claimed in the above-identified application.



U.S. Serial No.: 10/656,628  
Filing Date: September 5, 2003

Submission of the present document shall not be construed as an admission that a search has been made or that better art does not exist.

As far as is known to the undersigned, this Information Disclosure Statement is being filed within three months of the filing date of a national application, within three months of the date of entry of the national state in an international application, or before the mailing date of a first Office Action on the merits as set forth in 37 C.F.R. § 1.97(b), and therefore no fee is required.

While no fee is believed to be due, if this belief is in error the Commissioner is authorized to charge any additional fees, including extension fees or other relief which may be required, or credit any overpayment to Deposit Account No. 50-2319 (Our Order No. 463035-878 [A-71730/MSS]).

Please direct any calls in connection with this application to the undersigned at (650) 494-8700.

Respectfully submitted,  
DORSEY & WHITNEY LLP

Dated: 3-15-04

BY: Maria Swiatek  
Maria Swiatek, Reg. No. 37,244

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Attachments:

Form PTO/SB/8A-B (3 pgs.)  
24 References



<b>Substitute for form 1449A/PTO (Modified)</b>  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				<b>Complete if Known</b>	
				Application Number	10/656,628
				Filing Date	September 5, 2003
				First Named Inventor	Yoshihide SENZAKI
				Art Unit	2812
				Examiner Name	Not yet assigned
Sheet	1	of	3	Attorney Docket Number	A-71730/MSS

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.	Document Number Number-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	A1	4,239,811	12-16-1980	Kemlage	
	A2	4,720,395	01-19-1988	Foster	
	A3	5,032,545	07-1991	Doan et al.	
	A4	5,478,765	12-26-1995	Kwong et al.	
	A5	5,576,059	11-19-1996	Beinglass et al.	
	A6	5,578,848	12-26-1995	Kwong et al.	
	A7	5,744,196	04-28-1998	Laxman et al.	
	A8	5,874,368	02-23-1999	Laxman et al.	
	A9	5,932,286	08-03-1999	Beinglass et al.	
	A10	6,114,662	09-2000	Guidotti et al.	
	A11	6,150,286	11-21-2000	Sun et al.	
	A12	6,153,261	11-28-2000	Xia et al.	
	A13	2003-0104707 A1	06-05-2003	Senzaki	
	A14	2001-0003381 A1	06-14-2001	Orlowski et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.	Foreign Patent Document Country Code <sup>2</sup> Number <sup>4</sup> Kind Code <sup>5</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
	B1	EP 0 260 473 A1	03-23-1988	IBM		
	B2	EP 1 047 117 A2	10-25-2000	Oki Electric Ind. Co. Ltd.		

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Sheet	2	of	3	Attorney Docket Number	A-71730/MSS

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite <sup>1</sup> No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T <sup>3</sup>
	C1	Author Unknown, "Wafer Processing News: Nitride Gate Dielectric, Poly/W Electrode Enable 100nm CMOS", 2000, Cahners Semiconductor International, at <a href="http://www.semiconductor.net/semiconductor/issues/issues/2000/20001/six001wp.asp">http://www.semiconductor.net/semiconductor/issues/issues/2000/20001/six001wp.asp</a> , p. 1.		
	C2	ERIGUCHI, K., et al., "Role of Base Layer in CVD Si <sub>3</sub> N <sub>4</sub> Stack Gate Dielectrics on the Process Controllability and Reliability in Direct Tunneling Regime", <i>IEEE</i> , 1999, pp. 323-326.		
	C3	HENDA, R., et al., "Characterization of Chemically Vapor Deposited Silicon Nitride Films from Disilane and Ammonia", <i>Jpn. J. Appl. Phys.</i> , April 1, 1995, Vol. 34, Part 2, No. 4A: L437-L439.		
	C4	HENDA, R., et al., "Experimental and chemical kinetic study of silicon nitride via LPCVD at low temperature from disilane and ammonia", <i>Journal De Physique IV</i> , 1993, 3: 395-402.		
	C5	HENDA, R., et al., "Kinetics of the Low Pressure Chemical Vapor Deposition of Stoichiometric Silicon Nitride at Low Temperature from Disilane and Ammonia", <i>Journal of Chemical Vapor Deposition</i> , January 1993, 1: 300-314.		
	C6	KIM, B.Y., et al., "Ultra Thin (<3 nm) High Quality Nitride/Oxide Stack Gate Dielectrics Fabricated in In-Situ Rapid Thermal Processing", <i>IEEE</i> , 1997, pp. 463-466.		
	C7	LASER, A., et al., "Hot Wall Isothermal RTO for gate Oxide Growth and Nitridation", <i>Mat. Res. Soc. Meeting</i> , April 2000, Abstract C7.7.		
	C8	LAXMAN, R.K., et al., "A low-temperature solution for silicon nitride deposition", <i>Solid State Technology</i> , April 2000, 79-87.		
	C9	LEE, E., "Investigation of microstructure and grain growth of polycrystalline silicon deposited using silane and disilane", <i>Thin Solid Films</i> , 1993, 226:123-128.		
	C10	LEVY, S., et al., "Solutions for the 100nm Node with Ultrathin Silicon Nitride Gates", <i>Solid State Technology</i> , April 2001, pp. 75-80.		
	C11	MIZUNO, Y., et al., "Analysis of reaction gases flow in CVD processes", <i>Materials Science and Engineering</i> , 1995, B35: 156-159.		
	C12	OLIVARES, J., et al., "Effect of Deposition Parameters on the Characteristics of Low-Pressure Chemical Vapor Deposited SiGe Films Grown from Si <sub>2</sub> H <sub>6</sub> and GeH <sub>4</sub> ", <i>Journal of The Electrochemical Society</i> , 2001, 148(10):C685-C-689.		
	C13	ONAI, T., et al., "0.1 μm CMOS Technology for High-Speed Logic and System LSIs with SiO/Si/poly-Si/W Gate System", <i>IEEE</i> , 1999, pp. 937-938.		
	C14	SENZAKI, Y., et al., "Single-wafer furnace RTCVD for silicon oxide, nitride, and oxynitride thin films", <i>9<sup>th</sup> Int. Conference on Advanced Thermal Processing of Semiconductors</i> , RTP 2001 (Cat. No. 02EX513), Anchorage, Alaska, 25-29 Sept. 2001, pages 197-200.		
	C15	SONG, S.C., et al., "Ultra Thin (<20Å) CVD Si <sub>3</sub> N <sub>4</sub> Gate Dielectric for Deep-Sub-Micron CMOS Devices", <i>IEEE</i> , 1998, pp. 373-376.		
	C16	SONG, S.C., et al., "Ultra Thin High Quality Stack Nitride/Oxide Gate Dielectrics Prepared by In-Situ Rapid thermal N <sub>2</sub> O Oxidation of NH <sub>3</sub> -nitrided Si", republished in <i>Elsevier Science B.V., Microelectronic Engineering</i> , 1999, 48: 55-58.		
	C17	SONG, S.C., et al., "Ultra Thin High Quality Stack Nitride/Oxide Gate Dielectrics Prepared by In-Situ Rapid thermal N <sub>2</sub> O Oxidation of NH <sub>3</sub> -nitrided Si", <i>Symposium on VLSI Technology Digest of Technical Papers</i> , 1999, pp. 137-138.		
	C18	TANAKA, M., et al., "Film Properties of Low-k Silicon Nitride Films Formed by Hexachlorodisilane and Ammonia", <i>Journal of the Electrochemical Society</i> , 2000, 147(6): 2284-2289.		
	C19	TAYLOR, R.C., et al., "Hexachlorodisilane as a Precursor in the LPCVD of Silicon Dioxide and Silicon Oxynitride Films", <i>J. Electrochem. Soc.</i> , August 1989, 136(8): 2382-2385.		

Examiner Signature	Date Considered
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(Modified)**

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Sheet

**3**

of

**3**

Application Number

**10/656,628**

Filing Date

**September 5, 2003**

**First Named Inventor**

**Yoshihide SENZAKI**

Art Unit

2812

**Examiner Name**

**Not yet assigned**

Attorney Docket Number

**A-71730/MSS**

## NON PATENT LITERATURE DOCUMENTS

Examiner  
Initials\*Cite  
No.

Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.

 $T^6$ 

**C20**

TAYLOR, R.C., et al., "LPCVD of Silicon Nitride Films from Hexachlorodisilane and Ammonia", *Mat. Res. Soc. Symp. Proc.*, 1988, 105: 319-325.

C21

TEASDALE, D., et al., "LPCVD of silicon Nitride from Dichlorosilane and Ammonia by Single Wafer Rapid Thermal Processing", *Electrochemical and Solid State Letters*, The Electrochemical Soc., 2001, pp. F11-F12.

C22

YOON, T., et al., "Initial Stage of Amorphous Si and Si<sub>0.7</sub>Ge<sub>0.3</sub> Deposition on SiO<sub>2</sub> by Low-Pressure Chemical Vapor Deposition", *Journal of The Electrochemical Society*, 2002, 149(6): C301-C305.

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